

Connecting UniOP to the ABB 07KT97 Controllers

This Technical Note contains the information needed to connect UniOP to the ABB 07 KT 97 controllers.

The ABB 07 KT 97 supports communication via standard Modbus RTU protocol; this document describes the all steps necessary to establish a successful communication between uniOP and the controller using the “Modicon Modbus” communication driver contained in the UPLC5.DLL Designer file.

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1. Introduction

This ABB controller can be programmed to support communication with other devices as Modbus Slave or as Modbus Master.

The UniOP panel can act as Modbus Master and the PLC as Modbus Slave. The 07 KT 97 PLC has two COM ports with RS-232 interface that can be configured as required.

The following example shows all the steps required to connect UniOP to COM port 2, leaving COM port 1 to the connection with the programming software.

Note: Modbus protocol is active only when the PLC program is running. If both ports in the controller are configured to support the Modbus protocol, it is not possible to get any communication with the programming software until the PLC is switched in STOP mode.

2. Setting up the PLC for Communication

The MMI can be connected to 07 KT 97 only if an appropriate function block is called cyclically in the user program.

The following PLC program, it is an example that enables the Modbus Slave protocol on COM2 with ID 1.

The next table describes the variable declaration session.

```
PROGRAM PLC_PRG

VAR

    MODINIT_EN:           ARRAY[1..2] OF BOOL    := TRUE, TRUE; (*Release MODINIT*)
    MODBUS_IDENT:        ARRAY[1..2] OF INT     := 100,101;   (* Master/Slave Ident*)
    MODBUS_BAUD:         INT                    := 19200;     (*19200 baud*)
    MODBUS_PTY:          INT                    := 0;         (*no parity*)
    MODBUS_STOP:         INT                    := 1;         (*1 stop bit*)
    MODBUS_RTCTRL:       BOOL                   := FALSE;    (*no RTS control*)
    MODBUS_TLS:          INT                    := 0;         (*0 ms carrier lead time*)
    MODBUS_CDLY:         INT                    := 0;         (*0 ms carrier delay time*)
    MODBUS_CHTO:         INT                    := 3;         (*3 ms character timeout*)

    MODINIT_ERROR:       ARRAY[1..2] OF INT;      (*storage of errors*)

    MODINIT_COM2:        MODINIT;                (*instance*)

END_VAR
```

Figure 1 shows how the function block has to be called in the controller user program.

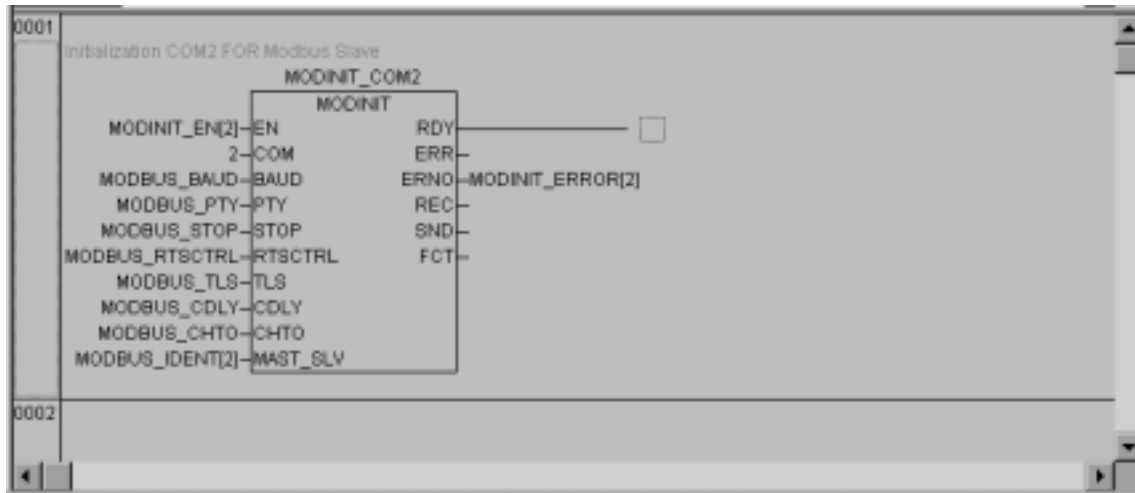


Figure 1

The example sets the communication parameters of UniOP like following:

Baud rate: 19200
Parity: None
Data bits: 8
Stop bits: 1

PLC slave id: 1

The ABB programming software version details are shown in Figure 2.



Figure 2

3. Cable Description

The UniOP panel can be connected via PLC port to the controller COM port using the following cable diagram.

PLC (9 Pin Male)			UNIOP (15 Pin Female)	
PGND	1	-----	1	Shield
TxD	2	-----	2	RxD
RxD	3	-----	3	TxD
SGND	7	-----	5	GND
RTS	6	---+		
CTS	8	---+		

4. Designer Configuration

The figure below shows the Designer Controller Setup dialog box for the Taian PLC. Slave ID contains the node number of the PLC connected to the operator panel.

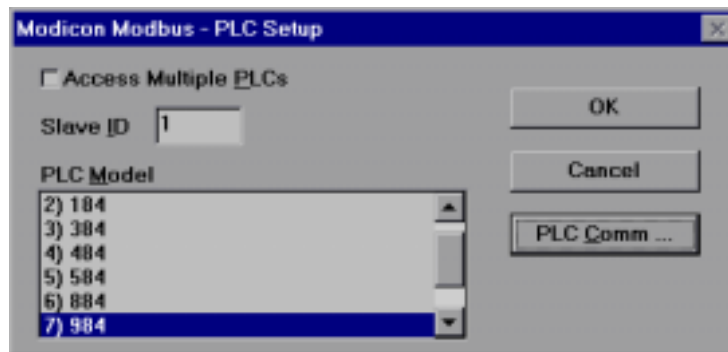


Figure 3 – Controller Setup dialog box

The protocol allows for multiple PLC's (max. 31 slaves) connected to one operator panel but only with a RS-232/RS-485 converter on all port RS-232 for all devices.

See Figure 4.

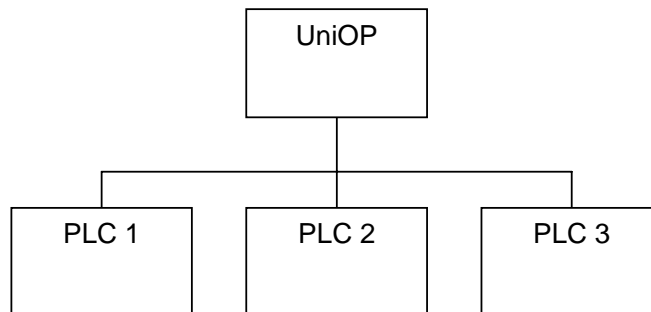


Figure 4

5. Controller Internal Resources Access

The internal memory area of the controller is mapped according to the rules explained in the following table.

Operand (symbolic)	Operand (IEC)	MODBUS address (Hex)	UniOP Driver Reference	Operand Description
INPUT				
E000_00 : E061_15	%IX000.00 : %IX061_15	0000 : 03DF	INP10001 : INP10992	Binary inputs, CS31 bus
E062_00 : E063_15	%IX062.00 : %IX063_15	03E0 : 03FF	INP10993 : INP11024	Binary inputs, local
E064_00 : E064_07	%IX064.00 : %IX064_07	0400 : 0407	INP11025 : INP11032	Binary inputs, local (binary access to EW006_00..EW006_07)
E065_00 : E099_15	%IX065.00 : %IX099_15	0410 : 063F	INP11041 : INP11600	Binary inputs, central expansion (reserved)
E100_00 : E163_15	%IX100.00 : %IX163_15	0640 : 0A3F	INP11601 : INP12624	Binary inputs, 2 nd non-central expansion (reserved)
E200_00 : E263_15	%IX220.00 : %IX263_15	0C80 : 0FFF	INP13201 : INP14096	Binary inputs, 3 rd non-central expansion (reserved)
OUTPUT				
A000_00 : A061_15	%QX000.00 : %QX061_15	1000 : 13DF	OUTP4097 : OUTP5088	Binary outputs, CS31 bus
A062_00 : A063_15	%QX062.00 : %QX063_15	13E0 : 13FF	OUTP5089 : OUTP5120	Binary outputs, local
A064_00 : A099_15	%QX064.00 : %QX099_15	1400 : 163F	OUTP5121 : OUTP5696	Binary outputs, central expansion (reserved)
A100_00 : A163_15	%QX100.00 : %QX163_15	1640 : 1A3F	OUTP5097 : OUTP6720	Binary outputs, 2 nd non-central expansion (reserved)
A200_00 : A255_15	%QX200.00 : %QX255_15	1C80 : 1FFF	OUTP7297 : OUTP8192	Binary outputs, 3 rd non-central expansion (reserved)
ANALOG INPUT				
EW000_00 : EW005_15	%IW1000.00 : %IW1005.00	0000 : 005F	HREG40001 : HREG40096	Analog inputs, CS31 bus

Operand (symbolic)	Operand (IEC)	MODBUS address (Hex)	UniOP Driver Reference	Operand Description
EW006_00 : EW006_07	%IW1006.00 : %IW1006.07	0060 : 0067	HREG40097 : HREG40104	Analog inputs, local
EW007_00 : EW007_14	%IW1007.00 : %IW1007.14	0070 : 007E	HREG40105 : HREG40127	Analog input (reserved)
EW007_15	%IW1007.15	007F	HREG40128	Analog input, status word CS31 bus
EW008_00 : EW015_15	%IW1008.00 : %IW1015.15	0080 : 00FF	HREG40129 : HREG40256	Analog inputs, CS31
EW016_00 : EW034_15	%IW1016.00 : %IW1034.15	0100 : 022F	HREG40257 : HREG40660	Analog inputs, central expansion (reserved)
EW100_00 : EW107_15	%IW1100.00 : %IW1107.15	0640 : 06BF	HREG41601 : HREG41728	Analog inputs, 1 st non-central expansion (reserved)
EW200_00 : EW207_15	%IW1200.00 : %IW1207.15	0C80 : 0CFF	HREG43201 : HREG43328	Analog inputs, 2 nd non-central expansion (reserved)
ANALOG OUTPUT				
AW000_00 : AW005_15	%QW1000.00 : %QW1005.00	1000 : 105F	HREG44097 : HREG44192	Analog outputs, CS31 bus
AW006_00 : AW006_07	%QW1006.00 : %QW1006.07	1060 : 1063	HREG44193 : HREG44196	Analog outputs, local
AW007_00 : AW007_14	%QW1007.00 : %QW1007.14	1070 : 107F	HREG44209 : HREG44224	Analog output (reserved)
AW008_00 : AW015_15	%QW1008.00 : %QW1015.15	1080 : 10FF	HREG44225 : HREG44352	Analog outputs, CS31 bus
AW016_00 : AW034_15	%QW1016.00 : %QW1034.15	1100 : 122F	HREG44353 : HREG44656	Analog outputs, central expansion (reserved)
AW100_00 : AW107_15	%QW1100.00 : %QW1107.15	1640 : 16BF	HREG45697 : HREG45824	Binary inputs, 1 st non-central expansion (reserved)
AW200_00 : AW207_15	%QW1200.00 : %QW1207.15	1C80 : 1CFF	HREG47297 : HREG47424	Binary inputs, 2 nd non-central expansion (reserved)
WORD FLAGS				
MW000_00 : MW1112_14	%MW1000.00 : %MW1112.14	2000 : 270E	HREG48193 : HREG49999	Word flags
MW1112_15 : :	%MW1112.15 : :	270F : :	HREG410000 : HREG412256	Word flags (supported by PLC but not with UnioP if a

Operand (symbolic)	Operand (IEC)	MODBUS address (Hex)	UniOP Driver Reference	Operand Description
MW1253_15	%MW1253.15	2FDF		standard Modicon Modbus driver it is used).
WORD FLAGS as bit				
M000_00 : M070_14	%MX0000.00 : %MX0070.14	2000 : 270E	HREG48193 : HREG49999	Word flags (bit access)
M070_15 : M254_15	%MX0070.15 : %MX0254.15	270F : 2FDF	HREG410000 : HREG412256	Word flags (bit access) (supported by PLC but not with UnioP if a standard Modicon Modbus driver it is used).
DOUBLE WORD FLAGS				
MD000_00 : MD063_15	%MD2000.00 : %MD2063.15	4000 : 43FF	HREG416387 : HREG417408	Double Word flags

Note: *the double word data format is swapped and it should be handled in the controller program*

Note: *Access to Binary Flags is not possible because they have the same Modbus Address as the Word Flags*
